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Performance Optimization and Tuning Techniques for IBM Power Systems Processors Including IBM POWER8 Brian Hall, Peter Bergner, Alon Shalev Housfater, Madhusudanan Kandasamy, Tulio Magno, Alex Mericas, Steve Munroe, Mauricio Oliveira, Bill Schmidt, Will Schmidt, Bernard King Smith, Julian Wang, Suresh Warriar, David Wendt, IBM Redbooks, 2017-03-31 This IBM® Redbooks® publication focuses on gathering the correct technical information, and laying out simple guidance for optimizing code performance on IBM POWER8® processor-based systems that run the IBM AIX®, IBM i, or Linux operating systems. There is straightforward performance optimization that can be performed with a minimum of effort and without extensive previous experience or in-depth knowledge. The POWER8 processor contains many new and important performance features, such as support for eight hardware threads in each core and support for transactional memory. The POWER8 processor is a strict superset of the IBM POWER7+™ processor, and so all of the performance features of the POWER7+ processor, such as multiple page sizes, also appear in the POWER8 processor. Much of the technical information and guidance for optimizing performance on POWER8 processors that is presented in this guide also applies to POWER7+ and earlier processors, except where the guide explicitly indicates that a feature is new in the POWER8 processor. This guide strives to focus on optimizations that tend to be positive across a broad set of IBM POWER® processor chips and systems. Specific guidance is given for the POWER8 processor; however, the general guidance is applicable to the IBM POWER7+, IBM POWER7®, IBM POWER6®, IBM POWER5, and even to earlier processors. This guide is directed at personnel who are responsible for performing migration and implementation activities on POWER8 processor-based systems. This includes system administrators, system architects, network administrators, information architects, and database administrators (DBAs).

Multicore Processors and Systems Stephen W. Keckler, Kunle Olukotun, H. Peter Hofstee, 2009-08-29 Multicore Processors and Systems provides a comprehensive overview of emerging multicore processors and systems. It covers technology trends affecting multicores, multicore architecture innovations, multicore software innovations, and case studies of state-of-the-art commercial multicore systems. A cross-cutting theme of the book is the challenges associated with scaling up multicore systems to hundreds of cores. The book provides an overview of significant developments in the architectures for multicore processors and systems. It includes chapters on fundamental requirements for multicore systems, including processing, memory systems, and interconnect. It also includes several case studies on commercial multicore systems that have recently been developed and deployed across multiple application domains. The architecture chapters focus on innovative multicore execution models as well as infrastructure for multicores, including memory systems and on-chip interconnections. The case studies examine multicore implementations across different application domains, including general purpose, server, media/broadband, network processing, and signal processing. Multicore Processors and Systems is the first book that focuses solely on multicore processors and systems, and in particular on the unique technology implications, architectures, and implementations. The book has contributing authors that are from both the academic and industrial communities.

Computational Mathematics and Applications Dia Zeidan, Seshadev Padhi, Aliaa Burqan, Peer Ueberholz, 2020-11-23 This book is a collection of invited and reviewed chapters on state-of-the-art developments in interdisciplinary mathematics. The book discusses recent developments in the fields of theoretical and applied mathematics, covering areas of interest to mathematicians, scientists, engineers, industrialists, researchers, faculty, and students. Readers will be exposed to topics chosen from a wide range of areas including differential equations, integral reforms, operational calculus, numerical analysis, fluid mechanics, and computer science. The aim of the book is to provide brief and reliably expressed research topics that will enable those new or not aware of mathematical sciences in this part of the world. While the book has not been precisely planned to address any branch of mathematics, it presents contributions of the relevant topics to do so. The topics chosen for the book are those that we have found of significant interest to many researchers in the world. These also are topics that are applicable in many fields of computational and applied mathematics. This book constitutes the first attempt in Jordanian literature to scientifically consider the extensive need of research development at the national and international levels with which mathematics deals. The book grew not only from the international collaboration between the authors but rather from the long need for a research-based book from different parts of the world for researchers and professionals working in computational and applied mathematics. This is the modified version of the back-cover content on the print book

Artificial Intelligence Applications and Reconfigurable Architectures Anuradha D. Thakare, Sheetal Umesh Bhandari, 2023-02-14 ARTIFICIAL INTELLIGENCE APPLICATIONS and RECONFIGURABLE ARCHITECTURES The primary goal of this book is to present the design, implementation, and performance issues of AI applications and the suitability of the FPGA platform. This book covers the features of modern Field Programmable Gate Arrays (FPGA) devices, design techniques, and successful implementations pertaining to AI applications. It describes various hardware options available for AI applications, key advantages of FPGAs, and contemporary FPGA ICs with software support. The focus is on exploiting parallelism offered by FPGA to meet heavy computation requirements of AI as complete hardware implementation or customized hardware accelerators. This is a comprehensive textbook on the subject covering a broad array of topics like technological platforms for the implementation of AI, capabilities of FPGA, suppliers' software tools and hardware boards, and discussion of implementations done by researchers to encourage the AI community to use and experiment with FPGA. Readers will benefit from reading this book because it serves all levels of students and researcher's as it deals with the basics and minute details of Ecosystem Development Requirements for Intelligent applications with reconfigurable architectures whereas current competitors' books are more suitable for understanding only reconfigurable architectures. It focuses on all aspects of machine learning accelerators for the design and development of intelligent applications and not on a single perspective such as only on reconfigurable architectures for IoT applications. It is the best solution for researchers to understand how to design and develop various AI, deep learning, and machine learning applications on the FPGA platform. It is the best solution for all types of learners to get complete knowledge of why reconfigurable architectures are

important for implementing AI-ML applications with heavy computations. Audience Researchers, industrial experts, scientists, and postgraduate students who are working in the fields of computer engineering, electronics, and electrical engineering, especially those specializing in VLSI and embedded systems, FPGA, artificial intelligence, Internet of Things, and related multidisciplinary projects.

Research Advances in Cloud Computing Sanjay Chaudhary,Gaurav Somani,Rajkumar Buyya,2017-12-28 This book addresses the emerging area of cloud computing, providing a comprehensive overview of the research areas, recent work and open research problems. The move to cloud computing is no longer merely a topic of discussion; it has become a core competency that every modern business needs to embrace and excel at. It has changed the way enterprise and internet computing is viewed, and this success story is the result of the long-term efforts of computing research community around the globe. It is predicted that by 2026 more than two-thirds of all enterprises across the globe will be entirely run in cloud. These predictions have led to huge levels of funding for research and development in cloud computing and related technologies. Accordingly, universities across the globe have incorporated cloud computing and its related technologies in their curriculum, and information technology (IT) organizations are accelerating their skill-set evolution in order to be better prepared to manage emerging technologies and public expectations of the cloud, such as new services.

Euro-Par 2014: Parallel Processing Fernando Silva,Inês Dutra,Vitor Santos Costa,2014-08-11 This book constitutes the refereed proceedings of the 20th International Conference on Parallel and Distributed Computing, Euro-Par 2014, held in Porto, Portugal, in August 2014. The 68 revised full papers presented were carefully reviewed and selected from 267 submissions. The papers are organized in 15 topical sections: support tools environments; performance prediction and evaluation; scheduling and load balancing; high-performance architectures and compilers; parallel and distributed data management; grid, cluster and cloud computing; green high performance computing; distributed systems and algorithms; parallel and distributed programming; parallel numerical algorithms; multicore and manycore programming; theory and algorithms for parallel computation; high performance networks and communication; high performance and scientific applications; and GPU and accelerator computing.

Non-Volatile Memory Database Management Systems Joy Arulraj,Andrew Pavlo,2022-06-01 This book explores the implications of non-volatile memory (NVM) for database management systems (DBMSs). The advent of NVM will fundamentally change the dichotomy between volatile memory and durable storage in DBMSs. These new NVM devices are almost as fast as volatile memory, but all writes to them are persistent even after power loss. Existing DBMSs are unable to take full advantage of this technology because their internal architectures are predicated on the assumption that memory is volatile. With NVM, many of the components of legacy DBMSs are unnecessary and will degrade the performance of data-intensive applications. We present the design and implementation of DBMS architectures that are explicitly tailored for NVM. The book focuses on three aspects of a DBMS: (1) logging and recovery, (2) storage and buffer management, and (3) indexing. First, we present a logging and recovery protocol that enables the DBMS to support near-instantaneous recovery. Second, we propose a storage engine architecture and

buffer management policy that leverages the durability and byte-addressability properties of NVM to reduce data duplication and data migration. Third, the book presents the design of a range index tailored for NVM that is latch-free yet simple to implement. All together, the work described in this book illustrates that rethinking the fundamental algorithms and data structures employed in a DBMS for NVM improves performance and availability, reduces operational cost, and simplifies software development.

Reversible Computation Simon Devitt,Ivan Lanese,2016-06-29 This book constitutes the refereed proceedings of the 8th International Conference on Reversible Computation, RC 2016, held in Bologna, Italy, in July 2016. The 18 full and 5 short papers included in this volume were carefully reviewed and selected from 38 submissions. The papers are organized in topical sections named: process calculi; reversible models; programming languages; quantum computing; quantum programming; circuit theory; and syntheses.

Corpus Presenter Raymond Hickey,2003 The manual contains many sample analyses and discussions so that users can acquaint themselves with the suite quickly and easily.--BOOK JACKET.

Distributed Computing Yoram Moses,2015-10-03 This book constitutes the proceedings of the 29th International Symposium on Distributed Computing, DISC 2015, held in Tokyo, Japan, in October 2015. The 42 full papers presented in this volume were carefully reviewed and selected from 143 submissions. The papers feature original contributions to theory, design, implementation, modeling, analysis, or application of distributed systems and networks. A number of 14 two-page brief announcements are included in the back matter of the proceedings.

Transactional Memory James R. Larus,Ravi Rajwar,2007-12-31 The advent of multicore processors has renewed interest in the idea of incorporating transactions into the programming model used to write parallel programs. This approach, known as transactional memory, offers an alternative, and hopefully better, way to coordinate concurrent threads. The ACI (atomicity, consistency, isolation) properties of transactions provide a foundation to ensure that concurrent reads and writes of shared data do not produce inconsistent or incorrect results. At a higher level, a computation wrapped in a transaction executes atomically – either it completes successfully and commits its result in its entirety or it aborts. In addition, isolation ensures the transaction produces the same result as if no other transactions were executing concurrently. Although transactions are not a parallel programming panacea, they shift much of the burden of synchronizing and coordinating parallel computations from a programmer to a compiler, runtime system, and hardware. The challenge for the system implementers is to build an efficient transactional memory infrastructure. This book presents an overview of the state of the art in the design and implementation of transactional memory systems, as of early summer 2006.

Computerworld ,1977-04-04 For more than 40 years, Computerworld has been the leading source of technology news and information for IT influencers worldwide. Computerworld's award-winning Web site (Computerworld.com), twice-monthly publication, focused conference series and custom research form the hub of the world's largest global IT media network.

Transactional Memory Tim Harris,James R. Larus,Ravi Rajwar,2010 The advent of multicore processors has renewed

interest in the idea of incorporating transactions into the programming model used to write parallel programs. This approach, known as transactional memory, offers an alternative, and hopefully better, way to coordinate concurrent threads. The ACI (atomicity, consistency, isolation) properties of transactions provide a foundation to ensure that con-current reads and writes of shared data do not produce inconsistent or incorrect results. At a higher level, a computation wrapped in a transaction executes atomically---either it completes successfully and commits its result in its entirety or it aborts. In addition, isolation ensures the transaction produces the same result as if no other transactions were executing concurrently. Although transactions are not a parallel programming panacea, they shift much of the burden of synchronizing and co-ordinating parallel computations from a programmer to a compiler, to a language runtime system, or to hardware. The challenge for the system implementers is to build an efficient transactional memory infrastructure. This book presents an overview of the state of the art in the design and implementation of transactional memory systems, as of early spring 2010.

Multicore Technology Muhammad Yasir Qadri,Stephen J. Sangwine,2018-10-08 The saturation of design complexity and clock frequencies for single-core processors has resulted in the emergence of multicore architectures as an alternative design paradigm. Nowadays, multicore/multithreaded computing systems are not only a de-facto standard for high-end applications, they are also gaining popularity in the field of embedded computing. The start of the multicore era has altered the concepts relating to almost all of the areas of computer architecture design, including core design, memory management, thread scheduling, application support, inter-processor communication, debugging, and power management. This book gives readers a holistic overview of the field and guides them to further avenues of research by covering the state of the art in this area. It includes contributions from industry as well as academia.

Best Practices for DB2 on AIX 6.1 for POWER Systems Rakesh Dash,Bernard Goelen,Vasfi Gucer,Rajesh K Jeyapaul,Sunil Kamath,Naveen Kumar Bharatha,Michael Kwok,Anupama Padmanabhan,Punit Shah,Basker Shanmugam,Sweta Singh,Amar Thakkar,Adriana Zubiri,IBM Redbooks,2015-08-27 This IBM® Redbooks® publication presents a best practices guide for DB2® and InfoSphere™ Warehouse performance on a AIX® 6L with Power Systems™ virtualization environment. It covers Power hardware features such as PowerVMTM, multi-page support, Reliability, Availability, and Serviceability (RAS) and how to best exploit them with DB2 LUW workloads for both transactional and data warehousing systems. The popularity and reach of DB2 and InfoSphere Warehouse has grown in recent years. Enterprises are relying more on these products for their mission-critical transactional and data warehousing workloads. It is critical that these products be supported by an adequately planned infrastructure. This publication offers a reference architecture to build a DB2 solution for transactional and data warehousing workloads using the rich features offered by Power systems. IBM Power Systems have been leading players in the server industry for decades. Power Systems provide great performance while delivering reliability and flexibility to the infrastructure. This book presents a reference architecture to build a DB2 solution for transactional and data warehousing workloads using the rich features offered by Power systems. It aims to demonstrate the benefits

DB2 and InfoSphere Warehouse can derive from a Power Systems infrastructure and how Power Systems support these products. The book is intended as a guide for a Power Systems specialist to understand the DB2 and InfoSphere Warehouse environment and for a DB2 and InfoSphere Warehouse specialist to understand the facilities available for Power Systems supporting these products.

Unique Chips and Systems Eugene John, Juan Rubio, 2018-10-08 Which came first, the system or the chip? While integrated circuits enable technology for the modern information age, computing, communication, and network chips fuel it. As soon as the integration ability of modern semiconductor technology offers presents opportunities, issues in power consumption, reliability, and form-factor present challenges. The demands of emerging software applications can only be met with unique systems and chips. Drawing on contributors from academia, research, and industry, Unique Systems and Chips explores unique approaches to designing future computing and communication chips and systems. The book focuses on specialized hardware and systems as opposed to general-purpose chips and systems. It covers early conception and simulation, mid-development, application, testing, and performance. The chapter authors introduce new ideas and innovations in unique aspects of chips and system design, then go on to provide in-depth analysis of these ideas. They explore ways in which these chips and systems may be used in further designs or products, spurring innovations beyond the intended scopes of those presented. International in flavor, the book brings industrial and academic perspectives into focus by presenting the full spectrum of applications of chips and systems.

Data Management on New Hardware Spyros Blanas, Rajesh Bordawekar, Tirthankar Lahiri, Justin Levandoski, Andrew Pavlo, 2017-03-21 This book contains selected papers from the 7th International Workshop on Accelerating Analytics and Data Management Systems Using Modern Processor and Storage Architectures, ADMS 2016, and the 4th International Workshop on In-Memory Data Management and Analytics, IMDM 2016, held in New Dehli, India, in September 2016. The joint Workshops were co-located with VLDB 2016. The 9 papers presented were carefully reviewed and selected from 18 submissions. They investigate opportunities in accelerating analytics/data management systems and workloads (including traditional OLTP, data warehousing/OLAP, ETL streaming/real-time, business analytics, and XML/RDF processing) running memory-only environments, using processors (e.g. commodity and specialized multi-core, GPUs and FPGAs, storage systems (e.g. storage-class memories like SSDs and phase-change memory), and hybrid programming models like CUDA, OpenCL, and Open ACC. The papers also explore the interplay between overall system design, core algorithms, query optimization strategies, programming approaches, performance modeling and evaluation, from the perspective of data management applications.

OpenMP: Advanced Task-Based, Device and Compiler Programming Simon McIntosh-Smith, Michael Klemm, Bronis R. de Supinski, Tom Deakin, Jannis Klinkenberg, 2023-08-30 This book constitutes the proceedings of the 19th International Workshop on OpenMP, IWOMP 2023, held in Bristol, UK, during September 13–15, 2023. The 15 full papers presented in this book were carefully reviewed and selected from 20 submissions. The papers are divided into the following topical sections: OpenMP and AI; Tasking Extensions; OpenMP Offload Experiences; Beyond Explicit GPU Support; and

OpenMP Infrastructure and Evaluation.

CFD Study on Hydrogen Engine Mixture Formation and Combustion Fushui Liu,2004

Proceedings of the Future Technologies Conference (FTC) 2019 Kohei Arai,Rahul Bhatia,Supriya Kapoor,2019-10-12

This book presents state-of-the-art intelligent methods and techniques for solving real-world problems and offers a vision of future research. Featuring 143 papers from the 4th Future Technologies Conference, held in San Francisco, USA, in 2019, it covers a wide range of important topics, including, but not limited to, computing, electronics, artificial intelligence, robotics, security and communications and their applications to the real world. As such, it is an interesting, exciting and inspiring read.

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